In the Claims

Please amend Claims 2, 5, 7-12, and 14-15.

A clean version of all the pending claims is submitted below:

1. A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer.

2. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor elevated above the regions in the fractional portion of the wafer.

3. A semiconductor packaging arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(C) a conductor for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

4. A method for providing a packaging arrangement, comprising:

providing a semiconductor wafer having formed thereon a plurality of semiconductor chips, such chips being separated by regions in the wafer, such wafer having a plurality of electrical contacts;

providing a dielectric member having thereon an electrical conductor;

positioning the dielectric member over the wafer with the electrical conductor being disposed on the plurality of electrical contacts and with such electrical conductor spanning the regions;

connecting the positioned dielectric member to the semiconductor wafer to provide a unitary structure;

separating the unitary structure into a plurality of packages, each one of packages having a plurality of the chips with the electrical contacts of the plurality of the chips in such package being electrically connected to a corresponding portion of the spanning electrical conductor in such package.

5. (Amended) The method recited in claim 4 including configuring electrical functionality of the assembly comprising:

selectively cutting the electrical conductor on the dielectric member and fusing selected regions of an interconnecting bus on the chips.

6. The method recited in claim 4 including providing a printed circuit board having an electrical interconnect thereon; and, electrically interconnecting the electrical conductor of the package to the electrical interconnect.

7. (Amended) A semiconductor memory, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region;

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the separating regions;

(B) an electrical interconnect for electrically connecting the array region of one of the chips to the periphery electrical component; and

(C) a fusible link disposed in the one of the memory array regions electrically connecting the electrical interconnect and the periphery electrical component.

8. A semiconductor memory, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region;

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the chips;

(B) an electrical interconnect for electrically connecting the array region of one of the chips to the periphery electrical component; and

(C) a fusible link disposed in one of the plurality of integrated circuit chips and electrically connecting the electrical interconnect and the periphery electrical component.

9. A semiconductor memory package, comprising:

(A) a fractional portion of a semiconductor wafer, such fractional portion having:

a plurality of integrated circuit chips, each one of such chips comprising:

a memory array region; and

wherein the chips have separating regions therebetween;

a periphery electrical component disposed in one of the separating regions;

(B) an electrical interconnect for electrically connecting the array region of the one of the chips to the periphery electrical component, such electrical interconnect elevated above the one of the separating regions.

10. (Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips having separating regions between them, the fractional portion of the wafer having a plurality of electrical contacts electrically connected to the chips;

an electrical conductor electrically connected to the plurality of electrical contacts to electrically interconnect such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer, such conductor elevated above the regions in the fractional portion of the wafer.

11. (Amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions between them; such fractional portion of the wafer having a plurality of electrical contacts electrically connected to the chips;

a dielectric having an electrical conductor thereon, such electrical conductor electrically connecting the plurality of electrical contacts to electrically interconnect such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

12. (Amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having:

a plurality of integrated circuit chips thereon, such chips have separating regions between them;

electrical components;

an electrical conductor for electrically connecting the plurality of electrical contacts to electrically interconnect such chips with the electrical components, such conductor elevated above the separating regions in the fractional portion of the wafer.

13. The package recited in claim 12 wherein the electrical components are disposed in the separating regions.

14. A semiconductor memory, comprising:

a fractional portion of a semiconductor wafer, such fractional portion of the wafer comprising:

a plurality of integrated circuit chips, each one of such chips having a memory array region;

separating regions between the chips;

a periphery electrical component disposed in one of the separating regions

an electrical interconnect for electrically connecting the chip to the periphery electrical component, such electrical interconnect elevated above one of the separating regions in the fractional portion of the wafer.

15. A semiconductor memory, comprising:

a fractional portion of a semiconductor wafer, such fractional portion of the wafer comprising:

a plurality of integrated circuit chips, each one of such chips having a memory array region, the chips have separating regions therebetween;

a peripheral electrical component disposed the one of the separating regions;

an electrical interconnect for electrically connecting the chip to the peripheral electrical component; and

a fusible link disposed in the one of the memory array regions and electrically connecting the electrical interconnect and the periphery electrical component.

16. A semiconductor module, comprising:

a printed circuit board having an electrical interconnect thereon; and

a semiconductor package mounted to the printed circuit board, such semiconductor package comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts electrically connected to the chips;

a dielectric having an electrical conductor thereon, such electrical conductor being electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips with portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

a connector for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

17. A method for providing a packing arrangement, comprising:

providing a semiconductor wafer having formed thereon a plurality of semiconductor chips, such chips being separated by regions in the wafer, such wafer having a plurality of electrical contacts electrically connected to the chips;

providing a dielectric member having an electrical conductor;

positioning the dielectric member over the wafer with the electrical conductor being disposed on the plurality of electrical contacts and with such electrical conductor spanning the regions; and

connecting the positioned dielectric member to the semiconductor wafer to provide a

unitary structure.

18. The method recited in claim 17 including separating the structure into a plurality of packages, each one of the of packages having a plurality of the chips with the electrical contacts of the plurality of the chips in such package being electrically connected to a corresponding portion of the spanning electrical conductor in such package.